

## S1C883 series Manual errata

ITEM AC Characteristics: External memory access						
Object manuals	Document code	Object pages				
S1C88348/317/316/308 technical manual	MF1183-02	I-156				
<b>(Error)</b>						
<ul style="list-style-type: none"> <li>• <b>Read cycle (Normal operating mode)</b></li> </ul>						
<i>Condition:</i> VDD = 2.4 to 5.5 V, VSS = 0 V, Ta = -40 to 85°C, VIH1 = 0.8VDD, VIL1 = 0.2VDD, VIH2 = 1.6 V, VIL2 = 0.6 V, VOH = 0.8VDD, VOL = 0.2VDD, CL = 100 pF (load capacitance)						
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in read cycle	tras	$t_c + t_1 - 100 + n \cdot t_c / 2$			nS	1
Address hold time in read cycle	trah	th-80			nS	
Read signal pulse width	trp	$t_c - 20 + n \cdot t_c / 2$			nS	1
Data input set-up time in read cycle	trds	300			nS	
Data input hold time in read cycle	trdh	0			nS	
Note) 1 Substitute the number of states for wait insertion in n.						
<ul style="list-style-type: none"> <li>• <b>Read cycle (High speed operating mode)</b></li> </ul>						
<i>Condition:</i> VDD = 3.5 to 5.5 V, VSS = 0 V, Ta = -40 to 85°C, VIH1 = 0.8VDD, VIL1 = 0.2VDD, VIH2 = 2.4 V, VIL2 = 0.9 V, VOH = 0.8VDD, VOL = 0.2VDD, CL = 100 pF (load capacitance)						
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in read cycle	tras	$t_c + t_1 - 50 + n \cdot t_c / 2$			nS	1
Address hold time in read cycle	trah	th-40			nS	
Read signal pulse width	trp	$t_c - 10 + n \cdot t_c / 2$			nS	1
Data input set-up time in read cycle	trds	150			nS	
Data input hold time in read cycle	trdh	0			nS	
Note) 1 Substitute the number of states for wait insertion in n.						

(Correct)

- **Read cycle (Normal operating mode)**

Condition:  $V_{DD} = 2.4$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -40$  to  $85^\circ\text{C}$ ,  $V_{IH1} = 0.8V_{DD}$ ,  $V_{IL1} = 0.2V_{DD}$ ,  $V_{IH2} = 1.6$  V,  $V_{IL2} = 0.6$  V,  $V_{OH} = 0.8V_{DD}$ ,  $V_{OL} = 0.2V_{DD}$ ,  $C_L = 100$  pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in read cycle	tr <sub>as</sub>	$t_c + t_1 - 100 + n \cdot t_c / 2$			nS	1
Address hold time in read cycle	tr <sub>ah</sub>	th-80			nS	
Read signal pulse width	tr <sub>p</sub>	$t_c - 20 + n \cdot t_c / 2$			nS	1
Data input set-up time in read cycle	tr <sub>ds</sub>	300			nS	<u>2</u>
Data input hold time in read cycle	tr <sub>dh</sub>	0			nS	

Note) 1 Substitute the number of states for wait insertion in n.

Note) 2. If tr<sub>ds</sub> is not satisfied, insert wait. (Refer to the wait control of 3.6.5)

- **Read cycle (High speed operating mode)**

Condition:  $V_{DD} = 3.5$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -40$  to  $85^\circ\text{C}$ ,  $V_{IH1} = 0.8V_{DD}$ ,  $V_{IL1} = 0.2V_{DD}$ ,  $V_{IH2} = 2.4$  V,  $V_{IL2} = 0.9$  V,  $V_{OH} = 0.8V_{DD}$ ,  $V_{OL} = 0.2V_{DD}$ ,  $C_L = 100$  pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in read cycle	tr <sub>as</sub>	$t_c + t_1 - 50 + n \cdot t_c / 2$			nS	1
Address hold time in read cycle	tr <sub>ah</sub>	th-40			nS	
Read signal pulse width	tr <sub>p</sub>	$t_c - 10 + n \cdot t_c / 2$			nS	1
Data input set-up time in read cycle	tr <sub>ds</sub>	150			nS	<u>2</u>
Data input hold time in read cycle	tr <sub>dh</sub>	0			nS	

Note) 1 Substitute the number of states for wait insertion in n.

Note) 2. If tr<sub>ds</sub> is not satisfied, insert wait. (Refer to the wait control of 3.6.5)