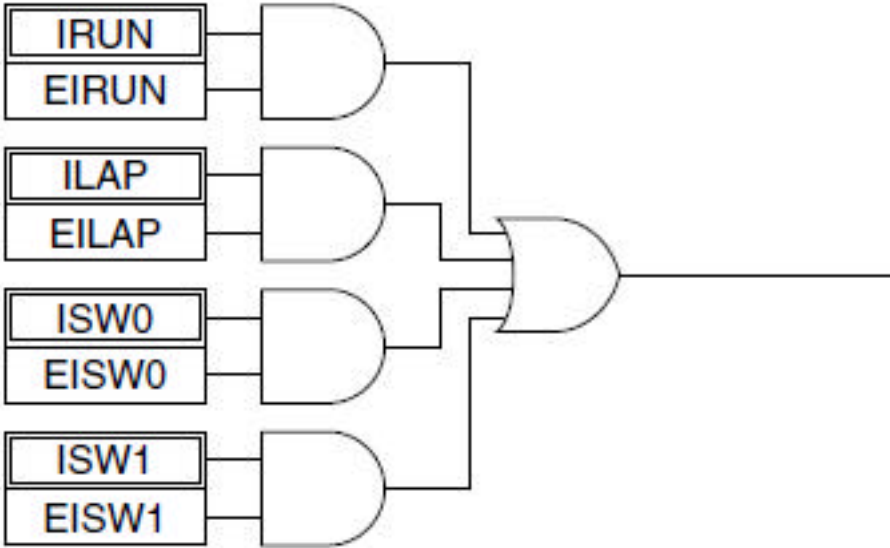
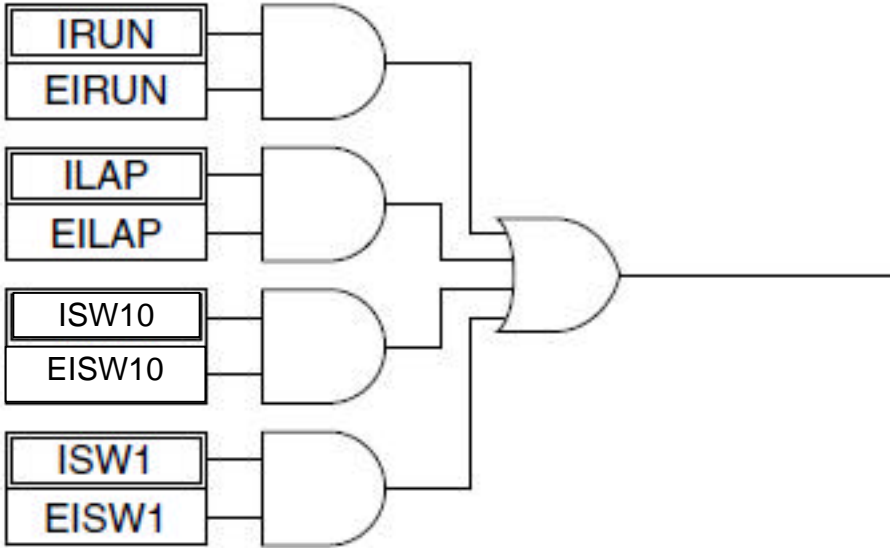


S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C63004/008/016 Technical Manual	411883700	5.6 Precautions	5-4
<p>(Error)</p> <ul style="list-style-type: none">• When a 3.0V LCD drive voltage is supplied to the VD3 or VD2 terminal in the 1.5V low-voltage type, use separated power sources for VDD and VD3/VD2 and supply a voltage within 1.1V to 1.7V to the VDD terminal.			
<p>(Correct)</p> <ul style="list-style-type: none">• When a 3.0V LCD drive voltage is supplied to the VC3 or VC2 terminal in the 1.5V low-voltage type, use separated power sources for VDD and VC3/VC2 and supply a voltage within 1.1V to 1.7V to the VDD terminal.			

S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C63004/008/016 Technical Manual	411883700	Figure 6.1.1 Configuration of the interrupt circuit	6-2
<p>(Error)</p> 			
<p>(Correct)</p> 			

S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C63004/008/016 Technical Manual	411883700	Note:	12-7
		12.8 Precautions	12-9
		I/O port	AP-D-3,4
<p>(Error)</p> <p>.....</p> <p>Make this waiting time the amount of time or more calculated by the following expression.</p> <p>$10 \times C \times R$</p> <p>C: terminal capacitance 5 pF + parasitic capacitance ? pF</p> <p>R: pull-down resistance 375 k (Max.)</p>			
<p>(Correct)</p> <p>.....</p> <p>Make this waiting time the amount of time or more calculated by the following expression.</p> <p>$10 \times C \times R$</p> <p>C: terminal capacitance 15 pF + parasitic capacitance ? pF</p> <p>R: pull-down resistance 500 k (Max.)</p>			

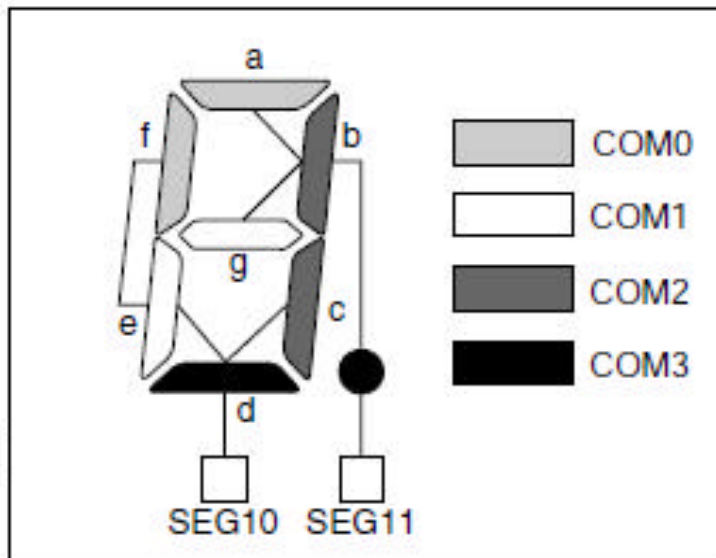
S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C63004/008/016 Technical Manual	411883700	13.6.4 SRDY signal	13-6
<p>(Error)</p> <ul style="list-style-type: none"> When negative polarity (SCPS1="1") is selected for the synchronous clock: The /SRDY signal goes "0" (low) when the S1C63004/008/016 serial interface is ready or receive data; normally, it is at "1" (high). The /SRDY signal changes from "1" to "0" immediately after "1" is written to SCTRГ and returns from "0" to "1" when "0" is input to the /SRDY (P30) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD[7:4], the /SRDY signal returns to "1". 			
<p>(Correct)</p> <ul style="list-style-type: none"> When negative polarity (SCPS1="1") is selected for the synchronous clock: The /SRDY signal goes "0" (low) when the S1C63004/008/016 serial interface is ready or receive data; normally, it is at "1" (high). The /SRDY signal changes from "1" to "0" immediately after "1" is written to SCTRГ and returns from "0" to "1" when "0" is input to the /SCLK (P30) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD[7:4], the /SRDY signal returns to "1". 			

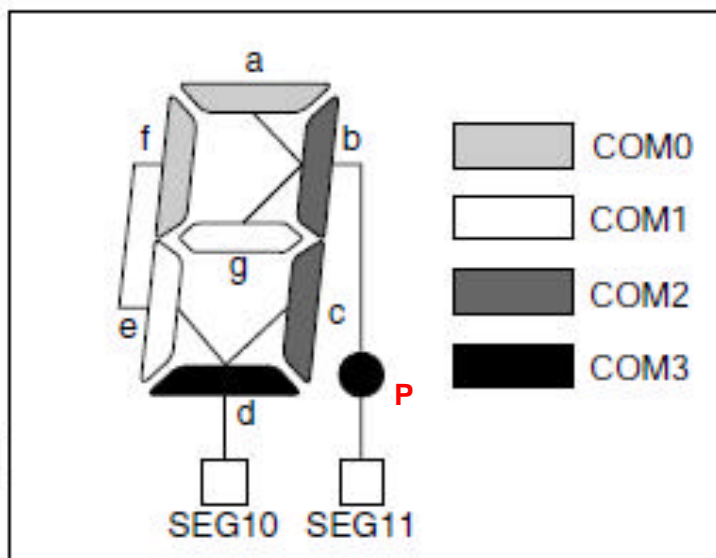
S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C63004/008/016 Technical Manual	411883700	Figure 14.2.3.1 Segment allocation	14-2

(Error)



(Correct)



S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C63004/008/016 Technical Manual	411883700	16.8 Precautions R/F converter	16-11 AP-D-4
(Error)			
(Correct) Add Reference/sensor oscillation frequency vs voltage deviation is increase for 1.5V low voltage type, please take into account this characteristic. Please refer to the RFC reference/sensor oscillation frequency – resistance characteristic at page from 19-14 to 19-15.			

S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C63004/008/016 Technical Manual	411883700	19.3 DC Characteristic	19-2
(Error)			
1.5 V low-voltage type			
Unless otherwise specified: $V_{DD}=1.1$ to $1.7V$, $V_{SS}=0V$, $T_a=-40$ to $85^{\circ}C$			
Item	Symbol	Condition	Min. Typ. Max. Unit
High level input voltage	V_{IH}	P00–P13 *1	$0.8V_{DD}$ – V_{DD} V
Low level input voltage	V_{IL}	P00–P13 *1	0 – $0.2V_{DD}$ V
High level Schmitt input voltage	V_{T+}	RESET, RFIN1, Pxx *2	$0.5V_{DD}$ – $0.9V_{DD}$ V
Low level Schmitt input voltage	V_{T-}	RESET, RFIN1, Pxx *2	$0.1V_{DD}$ – $0.5V_{DD}$ V
High level output current	I_{OH1}	$V_{OH1}=0.9V_{DD}$ Pxx, REF1, SEN1, HUD	– – -0.25 mA
Low level output current	I_{OL1}	$V_{OL1}=0.1V_{DD}$ Pxx, REF1, SEN1, HUD	0.25 – – mA
(Correct)			
1.5 V low-voltage type			
Unless otherwise specified: $V_{DD}=1.1$ to $1.7V$, $V_{SS}=0V$, $T_a=-40$ to $85^{\circ}C$			
Item	Symbol	Condition	Min. Typ. Max. Unit
High level input voltage	V_{IH}	P00–P13 *1	$0.8V_{DD}$ – V_{DD} V
Low level input voltage	V_{IL}	P00–P13 *1	0 – $0.2V_{DD}$ V
High level Schmitt input voltage	V_{T+}	RESET, RFIN1, Pxx *2	$0.5V_{DD}$ – $0.9V_{DD}$ V
Low level Schmitt input voltage	V_{T-}	RESET, RFIN1, Pxx *2	$0.1V_{DD}$ – $0.5V_{DD}$ V
High level output current	I_{OH1}	$V_{OH1}=0.9V_{DD}$ Pxx, REF1, SEN1, HUD	– – -0.25 mA
Low level output current	I_{OL1}	$V_{OL1}=0.1V_{DD}$ Pxx, REF1, SEN1, HUD	0.25 – – mA
High level Schmitt input voltage	Min. $0.5V_{DD}$	Min. $0.45V_{DD}$	
Low level Schmitt input voltage	Min. $0.5V_{DD}$	Min. $0.55V_{DD}$	

S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C63004/008/016 Technical Manual	411883700	20 Basic External Wiring Diagram	20-1

(Error)

Recommended values for external parts

Symbol	Name	Recommended value
X'tal	Crystal resonator	32.768 kHz
CG1	Trimmer capacitor	5 to 25pF
Ceramic	Ceramic resonator	4 MHz (3 V model) 1 MHz (1.5 V model)
CG3	Gate capacitor	30 pF (Ceramic oscillation)
CD3	Drain capacitor	30 pF (Ceramic oscillation)
C1	Booster capacitor	0.1 μ F
C2	Capacitor between VSS and VD1	0.1 μ F
C3	Capacitor between VSS and VOSC	0.1 μ F
C4	Capacitor between VSS and VC1	0.1 μ F
C5	Capacitor between VSS and VC2	0.1 μ F
C6	Capacitor between VSS and VC3	0.1 μ F
CP	Capacitor for power supply	3.3 μ F
Cres	Capacitor for RESET terminal	0.47 μ F

(Correct)

Recommended values for external parts

Symbol	Name	Recommended value
X'tal	Crystal resonator	32.768 kHz
CG1	Trimmer capacitor	0 to 25pF
Ceramic	Ceramic resonator	4 MHz (3 V model) 1 MHz (1.5 V model)
CG3	Gate capacitor	30 pF (Ceramic oscillation)
CD3	Drain capacitor	30 pF (Ceramic oscillation)
C1	Booster capacitor	0.1 μ F
C2	Capacitor between VSS and VD1	0.1 μ F
C3	Capacitor between VSS and VOSC	0.1 μ F
C4	Capacitor between VSS and VC1	0.1 μ F
C5	Capacitor between VSS and VC2	0.1 μ F
C6	Capacitor between VSS and VC3	0.1 μ F
CP	Capacitor for power supply	3.3 μ F
Cres	Capacitor for RESET terminal	0.47 μ F

S1C63 Manual errata

ITEM: Additional explanation and note about execution of SLP instruction			
Object manuals	Document codes	Items	Pages
S1C6F016	411801400	7.3 HALT and SLEEP	7-4
S1C63004/008/016	411883700	7.3 HALT and SLEEP	7-3
<p>(Error) - S1C6F016 (P7-4)、S1C63004/008/016 (P7-3)-</p> <p>SLEEP mode</p> <p>The CPU enters SLEEP mode when it executes the SLP instruction. In this mode, the CPU, and oscillation circuits (both OSC1 and OSC3) stop operating. Current consumption can considerably be reduced, as SLEEP mode stop all the peripheral circuits that operate with the internal clocks.</p> <p>The system can only be reactivated from SLEEP mode by a key input interrupt request from a P0x or P1x port.</p> <p>Therefore, set the following flag and the registers for the I/O port to be used to cancel SLEEP status before executing the SLP instruction.</p> <ul style="list-style-type: none"> • Interrupt flag (I flag) = "1" (interrupts are enabled) • Interrupt select register SIPxx = "1" (the Pxx I/O port interrupt is selected) • Interrupt mask register EIKxx = "1" (the Pxx I/O port interrupt is enabled) • Noise rejector select register NRSPxx = "00" (noise rejector is bypassed) 			

(Correct) - **S1C6F016 (P7-4)、 S1C63004/008/016 (P7-3)-**

SLEEP mode

The CPU enters SLEEP mode when it executes the SLP instruction. In this mode, the CPU, and oscillation circuits (both OSC1 and OSC3) stop operating. Current consumption can considerably be reduced, as SLEEP mode stop all the peripheral circuits that operate with the internal clocks. **To prevent improper operation after the CPU wakes up, be sure to run the CPU with the OSC1 clock before setting the CPU in the SLEEP mode.**

The system can only be reactivated from SLEEP mode by a key input interrupt request from a P0x or P1x port.

~~Therefore, set the following flag and the registers for the I/O port to be used to cancel SLEEP status before executing the SLP instruction.~~

- ~~• Interrupt flag (I flag) = "1" (interrupts are enabled)~~
- ~~• Interrupt select register SIPxx = "1" (the Pxx I/O port interrupt is selected)~~
- ~~• Interrupt mask register EIKxx = "1" (the Pxx I/O port interrupt is enabled)~~
- ~~• Noise rejector select register NRSPxx = "00" (noise rejector is bypassed)~~

Therefore, set and confirm the P0(1)x input level, the flag and the registers for the P0(1)x port and the CPU clock according to the following procedures to be used to enter / cancel SLEEP status before executing the SLP instruction surely.

1. CPU system clock switching register CLKCHG = "0" (OSC1 CPU clock is selected)
2. Interrupt selection register SIPxx = "1" (the P0(1)x input port interrupt is selected)
3. Interrupt mask register EIKxx = "1" (the P0(1)x input port interrupt is enabled)
4. Noise rejector selection register NRSPxx = "00" = "00" (noise rejector is bypassed)
5. Reset the P0(1)x input interrupt factor flag register (write "1" to the IKxx register)
6. Interrupt flag (I flag) = "1" (interrupts are enabled)
- 7-1. Confirm the input to the P0(1)x port is surely HIGH level when the P0(1)x port interrupt polarity select register = "1"(interrupt request signal is generated at the falling edge)
- 7-2. Confirm the input to the P0(1)x port is surely LOW level when the P0(1)x port interrupt polarity select register = "0"(interrupt request signal is generated at the rising edge)
8. Execute SLP instruction

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ITEM:			
Object manuals	Document codes	Items	Pages
S1C63004/008/016 Technical Manual	411883700	19.1 Absolute Maximum Rating 1.5 V low-voltage type	19-1

(Error)

Item	Symbol	...	Rated value	Unit
LCD power supply voltage	Vc3	...	-0.3 to <u>+3.0</u>	V

(Correct)

Item	Symbol	...	Rated value	Unit
LCD power supply voltage	Vc3	...	-0.3 to <u>+6.0</u>	V

S1C63 Manual errata

ITEM:			
Object manuals	Document codes	Items	Pages
S1C63004/008/016 Technical Manual	411883700	1.1 Features Table 1.1.1 Features of models	1-1
<p>(Error)</p> <p>Instruction execution time During operation at 4 MHz: 0.5 μsec 1 μsec <u>1.3 μsec</u></p>			
<p>(Correct)</p> <p>Instruction execution time During operation at 4 MHz: 0.5 μsec 1 μsec <u>1.5 μsec</u></p>			