

S1C33 Manual errata

ITEM Correction of pin setting explanation at PC-RS232Cboot mode

Object manuals	Document codes.	Item	Page
S1C33L26 Technical Manual	411900100	Configuration of PC RS232C Boot System	AP-D-6

(Error)

When the S1C33L26 is turned on or reset with the BOOT pin left open (or set to 1) and the #CE10 pin set to 0 (VSS), the S1C33L26 boots up by executing the MBR after loading it from the PC (RS232C) to IRAM via FSIO Ch.1.

Figure D.4.1.1 shows a PC RS232C boot system connection diagram.

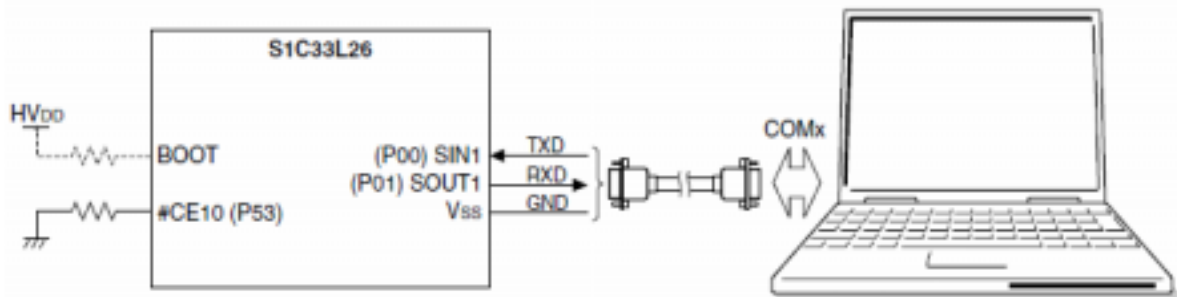


Figure D.4.1.1 PC RS232C Boot System

(Correct)

When the S1C33L26 is turned on or reset with the BOOT pin set to 1 (HVDD) and the #CE10 pin set to 0 (VSS), the S1C33L26 boots up by executing the MBR after loading it from the PC (RS232C) to IRAM via FSIO Ch.1.

Figure D.4.1.1 shows a PC RS232C boot system connection diagram.

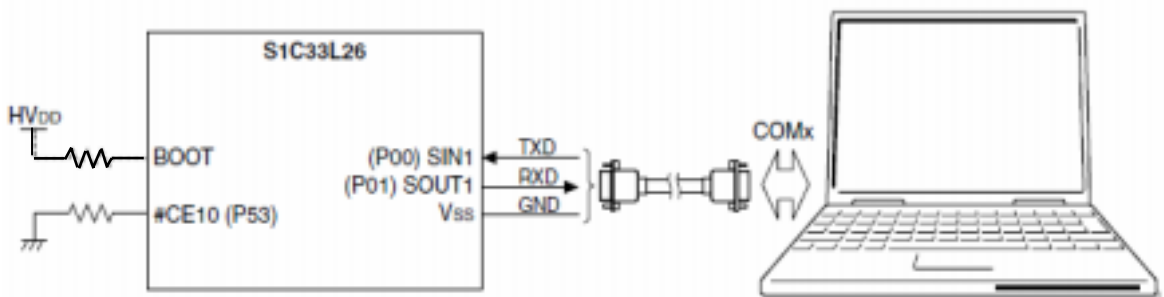


Figure D.4.1.1 PC RS232C Boot System

There is no internal pull-up resistor on the 'BOOT' pin.

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ITEM Correction of pin setting explanation at SPI boot mode			
Object manuals	Document codes	Item	Page
S1C33L26 Technical Manual	411900100	Configuration of SPI-EEPROM Boot System	AP-D-3
<p>(Error)</p> <p>When the S1C33L26 is turned on or reset with both the BOOT and #CE10 pins left open (or set to 1), the S1C33L26 boots up by executing the MBR after loading it from the EEPROM, FRAM, or Serial Flash connected to the SPI bus to IRAM.</p> <div style="text-align: center; margin: 10px 0;"> <p>The diagram shows the S1C33L26 microcontroller connected to an EEPROM (SPI). On the S1C33L26 side, the #CE10 (P53) and BOOT pins are connected to HVDD through pull-up resistors. The SPI interface pins are: P02 to #CS, (P03) USI_CK to CLK, (P01) USI_DO to D, and (P00) USI_DI to Q. Other pins include Pxx to #HOLD and #WP, and #RESET. A shared Reset signal is connected to #RESET on both devices. The EEPROM (SPI) side shows #HOLD and #WP pins connected to HVDD, and #RESET connected to the shared Reset signal.</p> </div> <p style="text-align: center;">Figure D.3.1.1 SPI-EEPROM Boot System</p>			
<p>(Correct)</p> <p>When the S1C33L26 is turned on or reset with both the BOOT and #CE10 pins set to 1(HVDD), the S1C33L26 boots up by executing the MBR after loading it from the EEPROM, FRAM, or Serial Flash connected to the SPI bus to IRAM.</p> <div style="text-align: center; margin: 10px 0;"> <p>The diagram shows the S1C33L26 microcontroller connected to an EEPROM (SPI). On the S1C33L26 side, the #CE10 (P53) and BOOT pins are connected to HVDD through pull-up resistors. The SPI interface pins are: P02 to #CS, (P03) USI_CK to CLK, (P01) USI_DO to D, and (P00) USI_DI to Q. Other pins include Pxx to #HOLD and #WP, and #RESET. A shared Reset signal is connected to #RESET on both devices. The EEPROM (SPI) side shows #HOLD and #WP pins connected to HVDD, and #RESET connected to the shared Reset signal.</p> </div> <p style="text-align: center;">Figure D.3.1.1 SPI-EEPROM Boot System</p>			

There is no internal pull-up resistor on 'BOOT' pin. Also in the sequence of SPI boot, the pull-up resistor of #CE10 is turned off, so that please add the external pull-up resistors to both 'BOOT' and '#CE10' pins.

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ITEM: Table correction of List of Other Pins										
Object manuals			Document codes		Items				Page	
S1C33L26 Technical Manual			411900100		Table 1.3.2.7 List of Other Pins				1-19	
(Error)										
Table 1.3.2.7 List of Other Pins										
NO.	Pin name	I/O	Description	Pin No.			PWR	DC characteristics		
				TQFP15 128	TQFP24 144	PFBGA 180		Input	Output	PU/PD
3	BOOT	I	Boot mode select signal input	6	6	D2	P2	LVCMOS Schmitt	-	50k PD
(Correct)										
Table 1.3.2.7 List of Other Pins										
NO.	Pin name	I/O	Description	Pin No.			PWR	DC characteristics		
				TQFP15 128	TQFP24 144	PFBGA 180		Input	Output	PU/PD
3	BOOT	I	Boot mode select signal input	6	6	D2	P2	LVCMOS Schmitt	-	-
<p>* There is no internal pull-down resistor on the 'BOOT' pin,</p>										