

S1C17 Family Technical Manual Errata

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(Error)

4.7 Precautions on Power Supply

Power-on sequence

In order to operate the device normally, supply power in accordance with the following timing.

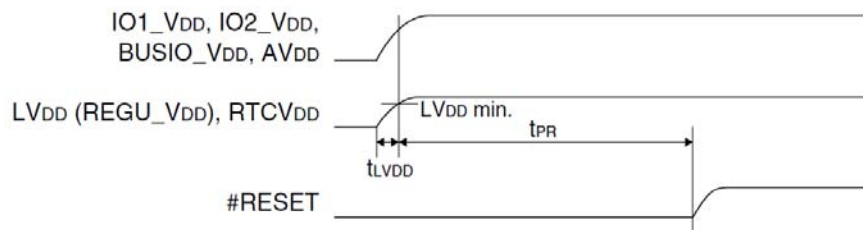


Figure 4.7.1 Power-On Sequence

(1) tLVDD: Elapsed time until the power supply stabilizes after power-on

Supply power in the following sequence.

Power-on: 1. LVDD (and RTCVDD) or REGU_VDD

2. BUSIO_VDD, IO1_VDD, IO2_VDD, AVDD (May be applied with 1 above at the same time.)

3. Apply the input signal

* The RTCVDD can be always supplied to the chip to operate the RTC and BBRAM.

(2) tPR: Power-on-reset time

Keep the #RESET signal low for this period. See “Electrical Characteristics” for the power-on-reset time.

(Correct)

4.7 Precautions on Power Supply

Power-on sequence

In order to operate the device normally, supply power in accordance with the following timing.

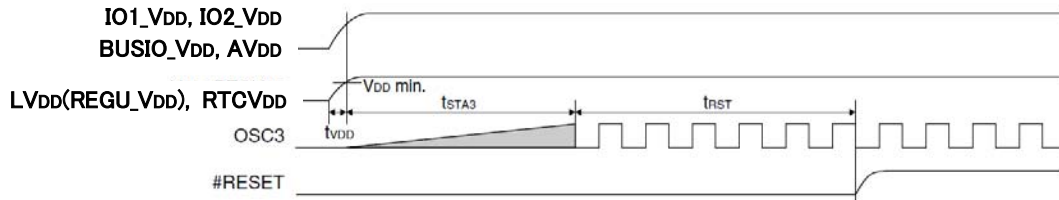


Figure 4.7.1 Power-On Sequence

- (1) t_{VDD} : Elapsed time until the power supply stabilizes after power-on

Supply power in the following sequence.

Power-on: 1. LV_{DD} (and RTCV_{DD}) or REGU_V_{DD}

2. BUSIO_V_{DD}, IO1_V_{DD}, IO2_V_{DD}, AV_{DD} (May be applied with 1 above at the same time.)

3. Apply the input signal

* The RTCV_{DD} can be always supplied to the chip to operate the RTC and BBRAM.

- (2) t_{STA3} : Time at which OSC3 oscillation starts

- (3) t_{RST} : Minimum reset pulse width

Time at which the clock supplied to the chip stabilizes plus at least six clocks; Keep the #RESET signal low.