

S1C17 Series Technical Manual Errata

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<p>(Error)</p> <p>D3 CBUFEN: Compare Buffer Enable Bit</p> <p>Enables or disables writing to the compare buffer.</p> <p>1 (R/W): Enabled</p> <p>0 (R/W): Disabled (default)</p> <p>Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare A and B buffers when the compare B signal is generated.</p> <p>Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.</p> <p>Note: Make sure the counter is halted (PRUN = 0) before setting CBUFEN.</p>			
<p>(Correct)</p> <p>D3 CBUFEN: Compare Buffer Enable Bit</p> <p>Enables or disables writing to the compare buffer.</p> <p>1 (R/W): Enabled</p> <p>0 (R/W): Disabled (default)</p> <p>Setting CBUFEN to 1 enables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B buffer values instead of the compare A and B register values. The compare A and B register values written via software are loaded to the compare</p>			

A and B buffers when the compare B signal is generated.

Setting CBUFEN to 0 disables the compare buffer. The compare A and B signals will be generated by comparing the counter values with the compare A and B register values.

Note: Make sure the counter is halted (**CLKEN** = 0) before setting CBUFEN.

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(Error)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated.

When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

Note: Make sure the counter is halted (**PRUN** = 0) before setting CBUFEN.

(Correct)

D3 CBUFEN: Compare Buffer Enable Bit

Enables or disables writing to the compare buffer.

1 (R/W): Enabled

0 (R/W): Disabled (default)

When CBUFEN is set to 1, compare data is written via the compare data buffer. The buffer contents are loaded into the compare A and compare B registers when the compare B signal is generated.

When CBUFEN is set to 0, compare data is written directly to the compare A and compare B registers.

Note: Make sure the counter is halted (**CLKEN** = 0) before setting CBUFEN.